IN THE CLAIMS:

1.-45. (Canceled)

46. (Original) A memory cell, comprising:

a plurality of transistors formed above a semiconducting substrate, each of said transistors comprised of a plurality of doped regions formed in said substrate; and

a plurality of local interconnects, each of which are conductively coupled to a doped region of one of said transistors and positioned in an opening in a layer of boron phosphosilicate glass (BPSG) and a dielectric layer positioned above said BPSG layer, said dielectric layer being comprised of a material having a dielectric constant greater than approximately 6.0.

47. (Original) The memory cell of claim 46, wherein said semiconducting substrate is comprised of silicon.

48. (Original) The memory cell of claim 46, wherein said doped regions are source/drain regions.

49. (Original) The memory cell of claim 46, wherein said BPSG layer has a thickness of approximately 150-200 nm.

50. (Original) The memory cell of claim 46, wherein said dielectric layer is comprised of at least one of aluminum oxide, tantalum pentoxide, hafnium oxide and zirconium oxide.

51. (Original) The memory cell of claim 46, wherein said local interconnect is comprised of at least one of a metal, a metal alloy, tungsten, copper, aluminum and polysilicon.

52. (Original) The memory cell of claim 46, wherein said dielectric layer has a thickness that ranges from approximately 300-850 nm.

53. (New) The memory cell of claim 46, wherein said dielectric layer is positioned on said BPSG layer.

54. (New) A memory cell, comprising:

a plurality of transistors formed above a semiconducting substrate comprised of silicon, each of said transistors comprised of a plurality of doped regions formed in said substrate; and

a plurality of local interconnects, each of which are conductively coupled to a doped region of one of said transistors and positioned in an opening in a layer of boron phosphosilicate glass (BPSG) and a dielectric layer positioned on said BPSG layer, said dielectric layer being comprised of a material having a dielectric constant greater than approximately 6.0.

55. (New) The memory cell of claim 54, wherein said doped regions are source/drain regions.

56. (New) The memory cell of claim 54, wherein said BPSG layer has a thickness of approximately 150-200 nm.

57. (New) The memory cell of claim 54, wherein said dielectric layer is comprised of at least one of aluminum oxide, tantalum pentoxide, hafnium oxide and zirconium oxide.

58. (New) The memory cell of claim 54, wherein said local interconnect is comprised of at least one of a metal, a metal alloy, tungsten, copper, aluminum and polysilicon.

59. (New) The memory cell of claim 54, wherein said dielectric layer has a thickness that ranges from approximately 300-850 nm.

60. (New) A memory cell, comprising:

a plurality of transistors formed above a semiconducting substrate comprised of silicon, each of said transistors comprised of a plurality of doped regions formed in said substrate; and

a plurality of local interconnects comprised of at least one of a metal, a metal alloy, tungsten, copper, aluminum and polysilicon, each of which are conductively coupled to a doped region of one of said transistors and positioned in an opening in a layer of boron phosphosilicate glass (BPSG) and a dielectric layer positioned

on said BPSG layer, said dielectric layer being comprised of at least one of aluminum oxide, tantalum pentoxide, hafnium oxide and zirconium oxide.

61. (New) The memory cell of claim 60, wherein said doped regions are source/drain regions.

62. (New) The memory cell of claim 60, wherein said BPSG layer has a thickness of approximately 150-200 nm.

63. (New) The memory cell of claim 60, wherein said dielectric layer has a thickness that ranges from approximately 300-850 nm.